UNIVERSITÄT PASSAU

Fakultät für Informatik und Mathematik

6092UE: Digital Design with Verilog-HDL on FPGA

Introduction; Basics; Topics

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Organization

- This seminar course is taught in English
- Fields of Study
  - Master Computer Science
  - Master AI Engineering (AISE)
  - Master Mobile and Embedded Systems
  - Bachelor students can also follow the theory parts if they wish
    - Bachelor Computer Science
    - Bachelor Internet Computing
- Focus Areas in Computer Science
  - IT-Security and Reliability
  - Intelligent Technical Systems
  - Information and Communication Systems
- **Participation to this exercise course is limited to 20 students**

- Stud.IP

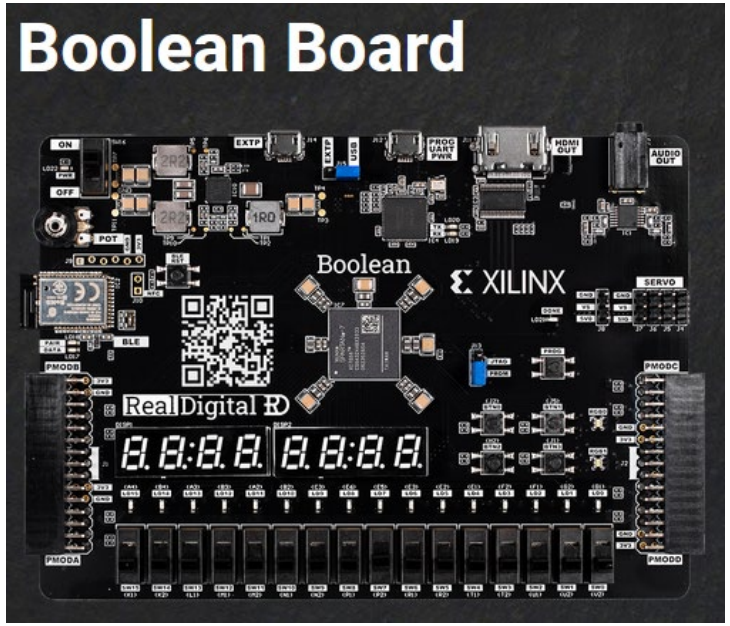
  Main communication point for the course!

Course Details

- No pre-requisites needed; but logic design, digital design, HDL knowledge would be plus
- Attendance to labs mandatory (except health problems with doctor's report)
  - Missing theoretical sessions can make it difficult to follow labs
- You will need to bring your own laptop for the lab sessions

- "Boolean board" will be provided for the lab sessions

- You need to download and install "Xilinx Vivado" software
  - You need to create a Xilinx account
  - Licenses will be provided for the labs through a license server
  - Or you can try the "30-Day trial" or "Free WebPack" options



Course Details

- For the theoretical sessions, we will meet in the designated classroom
    - Wednesdays 9:00 – 11:30 (with 15mins break)

- For the lab sessions we will meet on Wednesdays at the security lab at ITZ 102 (first floor)
    - There will be two groups of 10 students in the lab sessions
    - 2 students in a team will work together with one board
        - On separate laptops – let us know if you need to use the same laptop
    - First group. 8:30 – 9:45
    - Second group. 10:00 – 11:15

Lecture Organization and Timeline

- ***Week 1:*** Introduction, Basics, Short theoretical session
- ***Week 2:*** Theoretical session
- ***Week 3:*** Theoretical session
- ***Week 4:*** Lab session
- ***Week 5:*** Lab session
- ***Week 6:*** Lab session
- ***Week 7:*** Theoretical session
- ***Week 8:*** Theoretical session
- ***Week 9:*** Theoretical session
- ***3-Week Xmas Break***
- ***Week 10:*** Lab session
- ***Week 11:*** Lab session
- ***Week 12:*** Lab session
- ***Week 13:*** Lab session
- ***Week 14:*** Lab session

Assessment

- Portfolio Exam consists of
  - Lab results/reports handed in during the semester (50%)
    - Set 1 (20%)
    - Set 2 (30%)
  - Final assignment (50%)
    - Includes a final report submission
- Everyone will submit individually!

Course Content

- We will follow Boolean Board's provided lab content
  - https://www.realdigital.org/hardware/boolean
  - Example syllabus is available there
  - We will follow a slightly lighter version of that
    - This may also depend on the progress in the lab sessions

Topics

- Introduction to the Blackboard, Vivado, and Verilog
- Electric/electronic circuits; voltage, current, & power; power supplies
- Inputs and outputs, switch logic
- Diodes and transistors
- CMOS, logic gates and ICs
- Logic circuits, truth tables, representations, SOP & POS forms
- Logic equations, behavioral vs. structural, basic Verilog
- The case for minimization, overview of methods, and desired outcomes
- Boolean Algebra
- K-maps and don't cares
- Multiplexors, decoders, encoder, shifter/rotator
- Delays and glitches
- Electronic memory and basic cells
- Basic cells, registers, counters, latches, flip-flops
- Clock dividers, sequential circuit basics
- Controlling the Seven-Segment Display
- Arithmetic circuits: ripple-carry and carry-look ahead adders
- Negative numbers, encodings, and arithmetic implications
- Binary and 2’s complement subtractors
- Multipliers and Comparators
- Arithmetic and Logic Unit (ALU)
- Complete state diagrams, rules, and state codes
- Behavioral implementation of state machines in Verilog
- Stopwatch presentation: BCD counters, controller, and partitioning
- Structural implementations of state machines
- Reaction time monitor presentation: register files, simple filters
- Clock domains and clocking considerations
- Sampling and processing inputs
- Output signal timing issues

Registration

- In order to be considered for this exercise course
  - Please send an email to elif.kavun@uni-passau.de with shekoufeh.neisarian@uni-passau.de in cc
    - with **Digital Design with Verilog-HDL on FPGA WiSe2223** in the subject line
    - until **26.10.2022, 17:00**
    - Please respect the subject as your email will be filtered accordingly
  - Include the following information in your email as the students will be selected based on these criteria
    - Current semester of studies
    - Your transcript including your GPA and matriculation number
    - (Preferably) Your CV showing your experience and qualifications about logic/digital design, engineering, and computer science (not limited to these, please add any other relevant experience as well)
  - Read and act upon corresponding emails that you may receive later (if you are selected) for registration

Contact for Questions

- During the lecture/tutorials
  - Raise your hand during the lecture
  - Questions should be related to the course, not about another topic
- During the week
  - Please use *Stud.IP Forum* for questions!
    - So that your classmates can also learn from the discussions
    - Check the forum first, the question might already be answered
    - If not, post a new question
    - Questions should be related to the course, not about another topic
    - We will check at least every other day
- If you feel your question is personal/confidential
  - Send an email if the question is NOT of general interest

Thanks for your attention!

- Any questions or remarks?